Appl. No. 09/521,641

Amdt. dated April 28, 2004

Reply to Office Action of Oct. 29, 2003

## Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

## Listing of the Claims:

1 Claim 1 (currently amended): A method of performing

2 additive synthesis of digital audio signals in a recursive

3 digital oscillator, comprising:

receiving digital audio signal frames wherein each digital audio signal frame includes a set of frequency, amplitude, and phase components represented as coefficients of variables in a mathematical expression, each digital audio signal frame thereby including a frequency coefficient

representation;

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forming converted frequency coefficients by Re-Mapping linearaly re-mapping of bits of said frequency coefficient representation to bias audio reproduction accuracy toward low frequency signals; and

performing additive synthesis with said converted frequency coefficients.

1 Claim 2 (original): The method of claim 1 further

2 comprising the step of defining said frequency coefficient

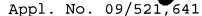
3 representation with an exponent characterizing a

4 floating-point range extension.

1 Claim 3 (currently amended): The method of claim 2 wherein

2 said defining step includes the step of specifying said

3 exponent to correspond to a right shift amount necessary to



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- 4 correct for precision limitations introduced by limiting
- 5 Re-Mapping re-mapping coefficients to 16 bits.
- 1 Claim 4 (original): The method of claim 3 wherein said
- 2 receiving, forming, and performing steps are implemented
- 3 utilizing a 16-bit fixed point processor.
- 1 Claim 5 (original): The method of claim 1 wherein said
- 2 receiving, forming and performing steps are implemented
- 3 utilizing a digital signal processor.
- 1 Claim 6 (original): The method of claim 1 wherein said
- 2 receiving, forming, and performing steps are implemented
- 3 utilizing a field programmable gate array.
- 1 Claim 7 (original): The method of claim 1 wherein said
- 2 receiving, forming, and performing steps are implemented
- 3 utilizing a Very Long Instruction Word processor.
- 1 Claim 8 (original): The method of claim 1 wherein said
- 2 receiving, forming, and performing steps are implemented
- 3 utilizing a Reduced Instruction Set Computer.
- 1 Claim 9 (original): The method of claim 1 wherein said
- 2 receiving, forming, and performing steps are implemented
- 3 utilizing a Residue Number System processor.
- 1 Claim 10 (currently amended): A computer readable memory to
- direct a processor to function in a specified manner,
- 3 comprising:

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a first set of executable instructions to receive digital audio signal frames wherein each digital audio signal frame has a set of specified frequency values expressed as a bit sequence;

a second set of executable instructions to Re-Map transform said bit sequence to represent lower frequencies with more significant bits and higher frequencies with less significant bits; and

a third set of executable instructions to facilitate additive synthesis of said digital audio signal frames in a reduced-precision recursive digital oscillator.

Claim 11 (original): The computer readable memory of claim 10 wherein said first set of executable instructions include instructions to identify a frequency coefficient representation of said specified frequency.

- Claim 12 (original): The computer readable memory of claim 11 further comprising a fourth set of executable instructions to define said frequency coefficient representation with an exponent characterizing a floating-point range extension.
- Claim 13 (currently amended): The computer readable memory of claim 12 wherein said fourth set of executable instructions include instructions to specify said exponent to correspond to a right shift amount necessary to correct for precision limitations introduced by a reduced reduce

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1 Claim 14 (new): A method of performing additive synthesis 2 of digital audio signals comprising:

- a) receiving a sequence of digital audio signal frames wherein each digital audio signal frame of said sequence includes a set of frequency, amplitude, and phase components; and,
- b) linearly scaling said amplitude component within each of said frames, frame N, wherein N labels a frame of said sequence, from zero to a peak value for a first portion of said frame N, and from said peak value to zero for a second portion of said frame N, creating thereby a scaled frame partial for frame N; and,
- c) summing successive scaled frame partials in a overlapping pairwise manner to produce a sequence of summed partials [N, (N+1)], [(N+1), (N+2)], [(N+2), (N+3)] continuing through at least a portion of said sequence, thereby approximating a varying-frequency varying-amplitude frame partial with a sum of two fixed-frequency fixed-amplitude scaled frame partials.
- 1 Claim 15 (new): A method as in claim 14 wherein said 2 overlapping pairwise summation comprises approximately 50% 3 overlap between members of each pair of said summed 4 partials.

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- Claim 17 (new): An oscillator as in claim 16 wherein  $\epsilon$  is represented by an unsigned mantissa, m, combined with an unsigned exponent, e, biased so that the actual represented value is  $\epsilon = 2^{2-e} m.$ 
  - 1 Claim 18 (new): An oscillator as in claim 17 wherein said 2 mantissa m is 16 bits.